EUROPEAN PATENT OFFICE

Patent Abstracts of Japan

PUBLICATION NUMBER : 56100514
PUBLICATION DATE : 12-08-81

APPLICATION DATE : 16-01-80
APPLICATION NUMBER : 55003979

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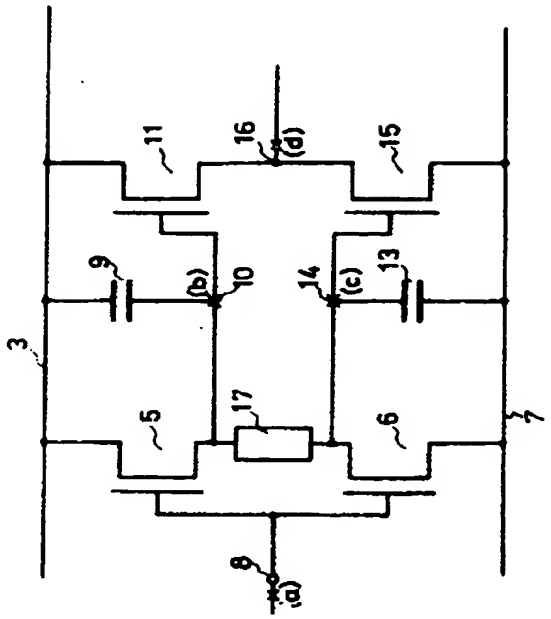
INT.CL. : H03H 11/26

TITLE : DELAY CIRCUIT



ABSTRACT : PURPOSE: To make the charging speed to the electrostatic capacity slow to prevent a through current, by providing an electric resistance at the connection point between the drain and the source of complementary FETs constituting the inverter of the first stage.

CONSTITUTION: Electric resistance 17 is provided at the connection point between the drain and the source of complementary FETs 5 and 6 constituting the inverter of the first stage. Then, the charging speed to electrostatic capacities 9 and 13 connected between high power source 3 and connection point 10 between the inverter of the first stage and the inverter of the next stage and between low power source 7 and connection point 14 between these inverters respectively becomes slow. Consequently, in respect to complementary FETs 11 and 15 constituting the inverter of the next stage, corresponding FETs 11 and 15 are not turned on simultaneously until the output voltage is changed. Therefore, a large through current is not generated, and power consumption is reduced.